FPGA based Embedded and Digital System Designing

Overview:

✓ Learn the essential basic and advance skills of FPGA base system designing using Verilog HDL
✓ Make your own system on chip by combining the power of parallelism and embedded processor
✓ Course is deeply practical and laboratory oriented

Who should attend?

✓ Engineering Students, Academic Persons and Fresh Graduates Engineers
✓ Students who wish to make their final year projects using this state of art technology
✓ Students in their first and second year are encouraged to attend

On completion, participants will be able to:

✓ Construct complete Verilog HDL models
✓ Make their projects using this state of art technology
✓ Make themselves valuable resource for the industry
✓ Implement complex and high speed designs like Bitcoin Mining, Software Defined Radios, Real Time Image Processing, High Speed Communication Systems, Aerospace and Defense Systems
✓ Simulate, test and troubleshoot their designed Verilog HDL models

Course Outline:

✓ Digital Logic Design Basics (Flip Flops, Combinational and Sequential Circuits, Propagation Delays etc.)
✓ Evolution of Programmable Devices
✓ Introduction to FPGA
✓ Features & Advantages of FPGA
✓ FPGA Device Families Architecture
✓ FPGA Design Flow
✓ FPGA in-depth comparison with ASIC and Microcontrollers
✓ FPGA Applications and Scope
✓ Introduction to Verilog HDL
✓ Verilog HDL Architecture
✓ Verilog HDL Lexical Convention and types of Lexical Tokens
✓ In-depth study of Gate Level, Data Flow and Behavioral Modeling
✓ Design errors and their remedy
✓ State Machine Design Concept
✓ Test & Verification Methodologies
✓ Familiarization with Modelsim Simulation tool
✓ Synthesis & Analysis, Place & Route, and Implementation
✓ Hardware Testing of FPGA Based Design
✓ Using the Altera Monitor Program
✓ Using the SignalTap II Logic Analyzer
✓ Probing the Design Using SignalTap in real time
Projects, Labs and Assignments:

- Designing multi bits multiplexers, comparators, using Gate Level Modeling and perform its simulation on Modelsim
- BCD to Seven Segment Decoder
- Parameterized Clock Divider Module
- 16-bit Parallel in serial out and serial in parallel out core
- Design a 32-bit one hot ring-counter
- Up and Down Counter with Load and Preset functionality
- Designing an ALU with 32-bit inputs and outputs
- Implementing an 8x64 FIFO buffer with read and write ports of the FIFO operating at the same clock. Generate control signals to indicate the FIFO full/empty conditions
- Real time Traffic Signal Controller
- State machine to detect any given sequence like ‘101’ from an incoming serial stream
- State machine to detect divisible by 5 value in an input serial stream of any length
- Interfacing Character LCD and making digital clock, visual menus, welcome screens
- Implementing Serial Communication Protocol (UART transmitter/receiver) and communicating with computer running graphic user interface

Course Information:

Duration: 24hrs

Venue: Usman Institute of Technology

Timings: Every Saturday from 2:00 p.m-4:00 p.m and Sunday from 10:00 a.m - 12:00 p.m

Course Fee: Rs. 7,000/=  

Material and Resources:

Participants will get all the presentations, lab manuals, tutorials and software provided by the trainer